In the Claims

1. (original) A semiconductor processing method of forming integrated circuitry comprising:

forming memory circuitry and peripheral circuitry over a substrate, the peripheral circuitry comprising first and second type MOS transistors; and

conducting second type halo implants into the first type MOS transistors in less than all peripheral MOS transistors of the first type.

2. (original) The semiconductor processing method of claim 1, wherein the second type is p-type.

3. (original) The semiconductor processing method of claim 1, wherein the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

4. (original) The semiconductor processing method of claim 1, wherein:

the second type is p-type; and

the conducting of the second type halo implants comprises conducting said implants into only one of the source and drain regions in the less than all of the peripheral MOS transistors of the first type, and not the other of said source and drain regions of said less than all of the peripheral MOS transistors of the first type.

Claims 5-15 (cancelled)

16. (currently amended) A semiconductor processing method comprising:

~~In~~ a ~~common~~ masking step providing a common mask; and

~~in a common~~ an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, at least some of the devices forming memory access devices.

17. (currently amended) The method of claim 16, wherein the at least some of the devices forming memory access devices receive halo implants on a ~~bitline~~ bit line contact side of the devices.

Claims 18-40 (cancelled)

41. (original) A method of improving DRAM storage cell retention time comprising conducting, in a common masking step and in a common implant step, a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to each device one of two or more different respective threshold voltages, at least some of the devices forming memory access devices, wherein the at least some of the devices forming memory access devices receive halo implants on a bit line contact side of the devices.

42. (original) The method of claim 41 wherein the halo implant is performed prior to formation of sidewall spacers in the memory access devices.

43. (original) The method of claim 41 wherein the halo implant is performed after formation of sidewall spacers in the memory access devices.

44. (original) The method of claim 41 wherein the halo implant is accompanied with an n-minus implant on the bit line contact side.

45. (currently amended) The method ~~of~~ of claim 41 wherein the storage node side of the memory access device is masked from the halo implant.

46. (currently amended) A method of improving DRAM storage cell retention time comprising forming memory access devices having different implants and hence different junction structures on a ~~bitline~~ bit line contact side and a storage node side respectively.

47. (currently amended) The method of claim 46 wherein forming memory access devices includes:

performing, during a masking and implant step, a one-sided halo implant on the ~~bitline~~ bit line contact side; and

performing, during the masking and implant step, an n-minus implant on the ~~bitline~~ bit line contact side.

48. (original) The method of claim 47, wherein performing a one-sided halo implant is performed prior to formation of sidewall spacers.

49. (currently amended) The method of claim 46, wherein the storage node side is masked during a one-sided halo implant on the ~~bitline~~ bit line contact side.